

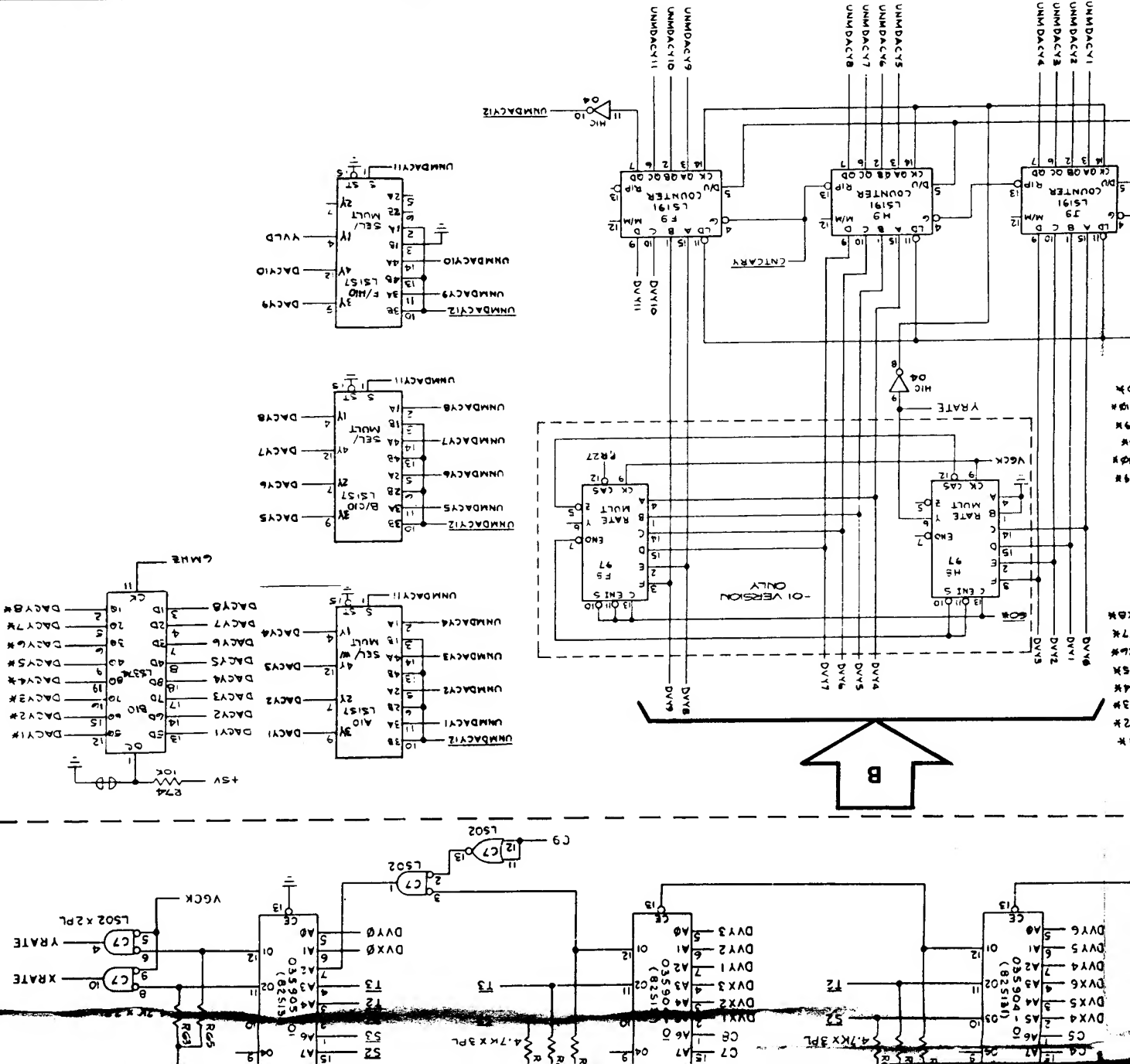
# Section of 036471-01 and -02 Video Generator ASTEROIDS DELUXE™ Sheet 2, Side A

A Warner Communications Company



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DACX1 thru UNMDACX10 (X-axis unmultiplexed digital-to-  
 analog converter circuitry). The DACX1 thru DACX10 signals are  
 transferred on each rising edge of the 6-MHz clock (from the  
 digital-to-analog converters (DACs) in the X video output.  
 DACX1 and DACX10 outputs represent the physical placement  
 of the screen and start again on the left side of the  
 "wraparound" condition. To prevent a wraparound, the  
 "select input from UNMDACX11 goes high when the  
 counter is 1023 or less than 0. This selects UNMDACX12 to  
 from the multiplexers to the DACs, forcing all zeros or all  
 ones keeping the beam on the appropriate side on the  
 read of allowing it to wraparound.  
 and VLD (X and Y valid) outputs from the X- and  
 counter multiplexers are latched (F10) and gated together to  
 axis output, BVL (beam valid).



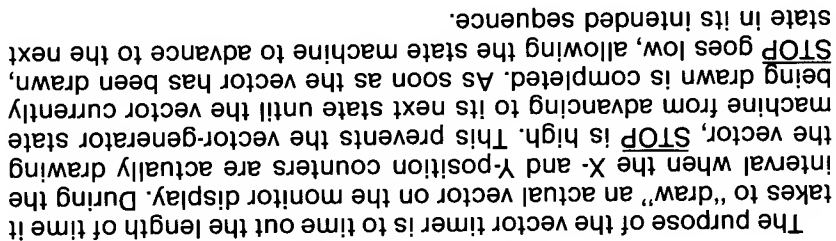
.....



erator causes LDSTROBE to go low. At this time, a new

vector being drawn.

A diagram of a right-pointing arrow. Inside the arrow, the letter 'B' is written. To the left of the arrow, the text 'T. 1' is written vertically.



If the TIMER signals are all high, ALPHANUM goes low and data signals DVX11 and DVT11 are decoded by decoder E6. This is added to the scale factor and loaded into the counters.

The X- and Y-positions of the beam are determined by the X- and Y-positions of the beam on the screen. The X- and Y-positions of the beam on the screen are determined by the X- and Y-positions of the beam on the screen. The X- and Y-positions of the beam on the screen are determined by the X- and Y-positions of the beam on the screen.

During initial power-up of the game, the HALT signal is pre-set low. The microcomputer reads the high HALT signal through its switch input port (sel/mux L10) on data line DB7. This tells the microcomputer that the vector generator is halted and waiting for an instruction. To ensure that the beam is off when the state machine is halted, the high HALT, clocked through latch D8, results in a low BLANK to the Z-axis output.

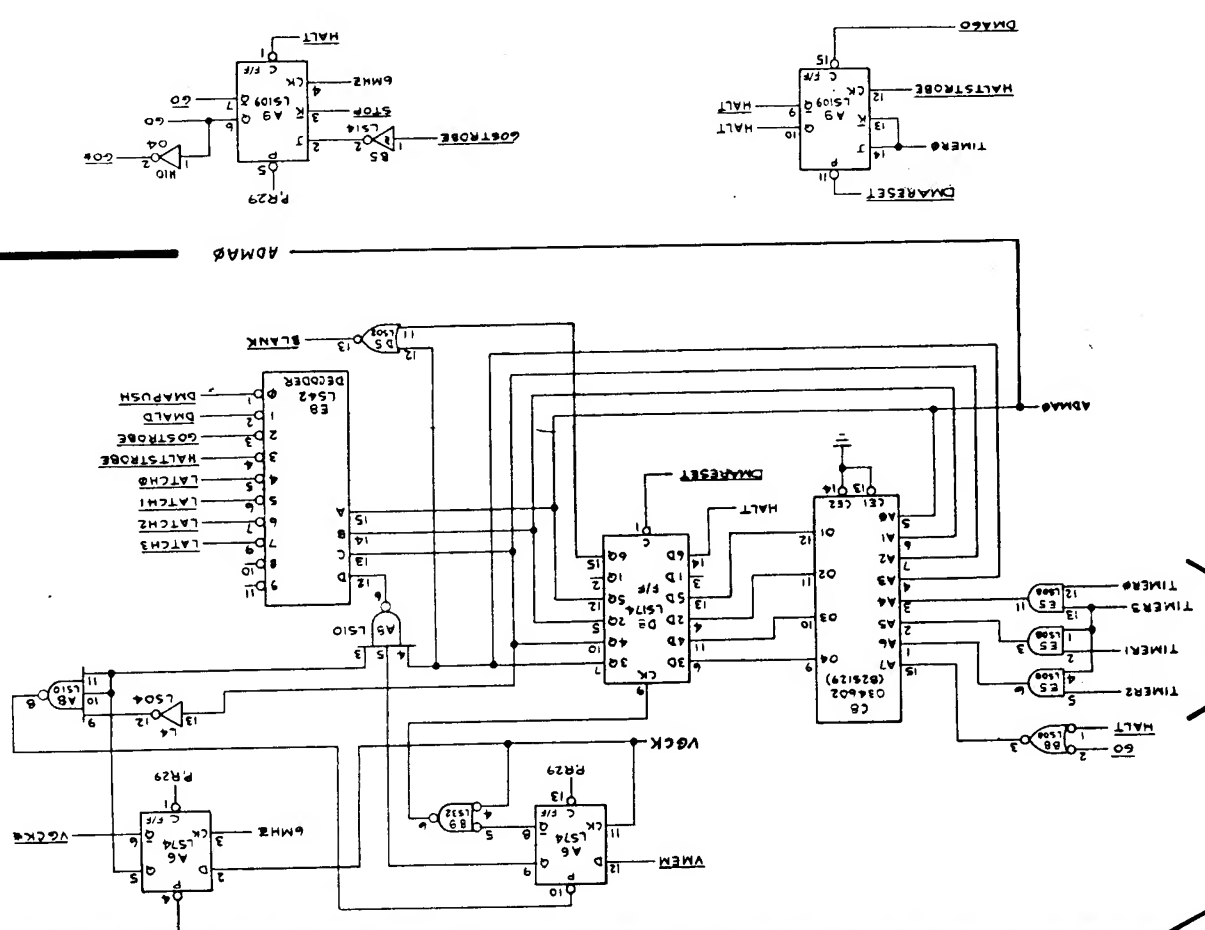
The state machine consists of input gates B8 and E5, ROM C8, latch D8, clock circuitry A6, and decoder E8. Four-bit input TIMER0 thru TIMER3 is the operation-code input to the state machine. The A4 thru A6 address input to ROM C8 tells the ROM which instructions to perform. Address inputs A0 thru A3 from latch D8 tells the ROM which state was last performed. The address A7 input GO tells the ROM that the position counters are presently drawing a vector. The HALT input to A7 tells the ROM that the vector generator has completed its operations.

The state machine is the "master controller" of the vector generator circuitry. It receives instructions from the game MPU, via the vector generator RAM. It carries out these instructions by accessing the appropriate sections of the vector-generator ROM memory, using the vector-generator program counter to do so. The state machine reads the vector-generator ROM data (via Timer 0-3) and decodes this information to determine how it should use this data: 1) to draw a vector, 2) to move the monitor beam to a new position on the monitor display, 3) to "jump" to a new vector memory address, 4) to return to a previous vector memory address, or 5) to tell the game MPU that it has completed its current instructions, and is waiting for its next command.

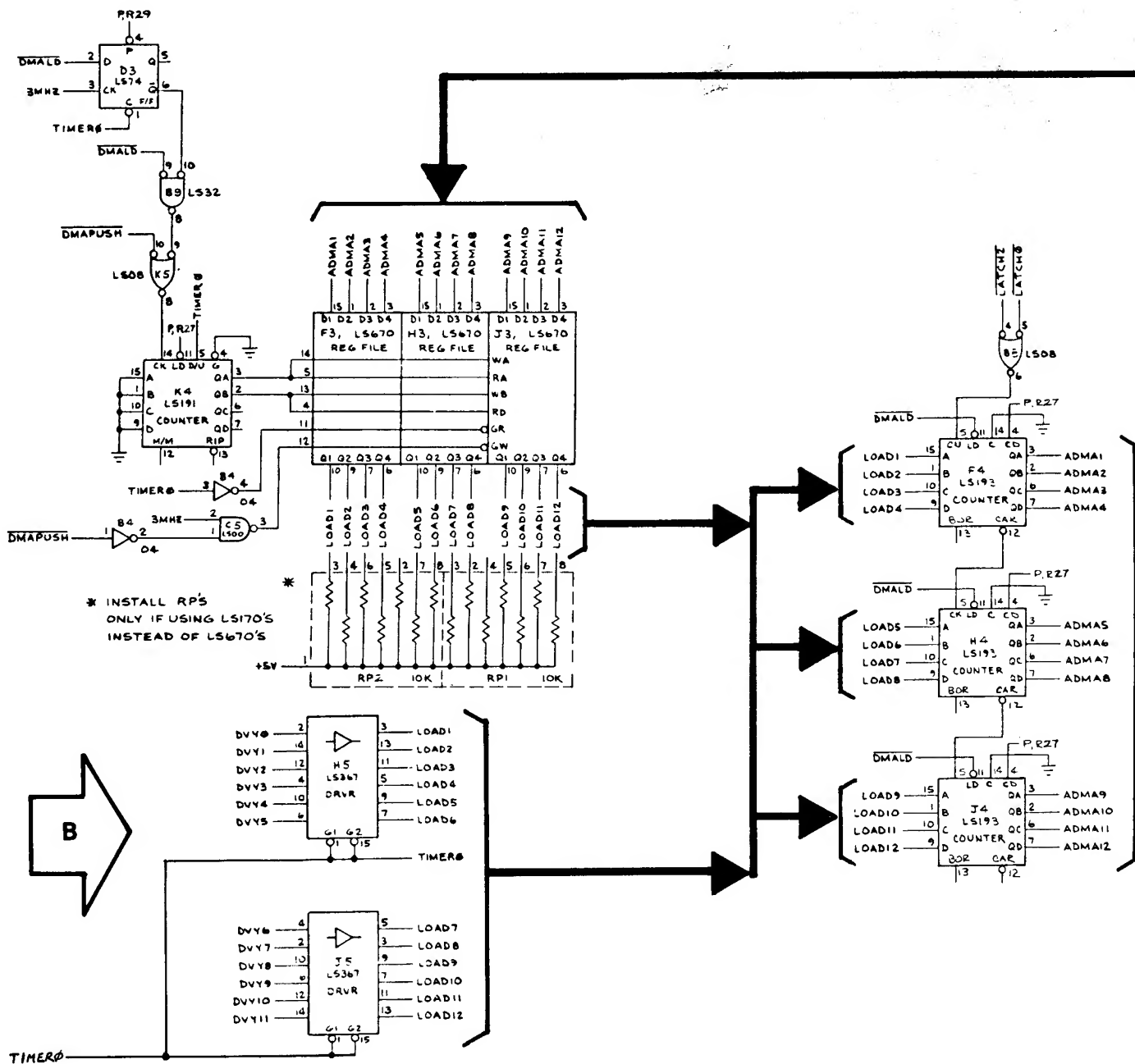
The VGCK input to the clock circuitry is a buffered 1.5MHz clock signal from the microcomputer. This is the same frequency used to clock the MPU of the microcomputer. The signal clocks latch D8 unless the microcomputer is addressing the vector RAM or ROM memories (when VMEM goes low). Then the clock input to latch D8 goes high and stays high until VMEM goes high.

The GO signals load and enable the vector timer and the X and Y position counters and tell the ROM that the vector generator is now actively drawing a vector. The HALT input to GO flip-flop A9 sets the outputs to ensure that the vector timer and position counters are not active when the state machine is halted. When a low GOSTROBE is clocked through A9, the vector timer and X- and Y-position counters begin to operate from the GO, GO and GO\* signals. When STOP is clocked through A9, the vector timer has reached its maximum count, and GO goes high. This means the vector has been drawn.

When the state machine receives the operation code for a HALT instruction, it outputs a low HALTSTROBE, setting the HALT flip-flop A9, and suspending state machine operation. The microcomputer outputs an address that results in a DMAGO signal that causes HALT to go high, and clears the vector-generator data latches. This makes TIMER0 thru TIMER3 signals all low. The state machine now begins executing instructions, starting at vector memory location 0.



# PROGRAM COUNTER

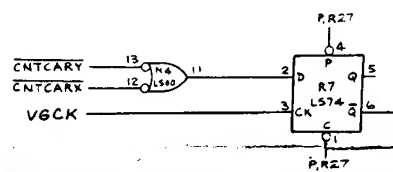
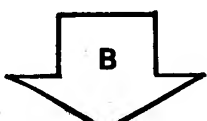


Counters F4, H4 and J4 contain the address of the next data byte (instruction) to be fetched from the Vector Generator memory. Because these counters point to the next instruction in memory to be retrieved and performed, they are called the program counter. This program counter is incremented one count (to the next sequential address) each time the information at its current address is loaded into data latch 0 or data latch 2.

The program counter may also be preset to "jump" to a new address. This new address can be loaded into the program counter from the vector generator memory via data latches F6 and H6 and buffers H5 and J5.

The program counter may also be preset to "return" to a previous address which it had stored in its "stack". The stack consists of register files F3, H3, & J3, and down/up counter K4. The stack is a 4-word 12-bit memory, used to save the contents of the program counter for future reference. It is loaded when DMAPUSH is low. Immediately after information is written into the stack, counter K4 increments one count. Immediately before loading the program counter from the stack, counter K5 decrements one count.

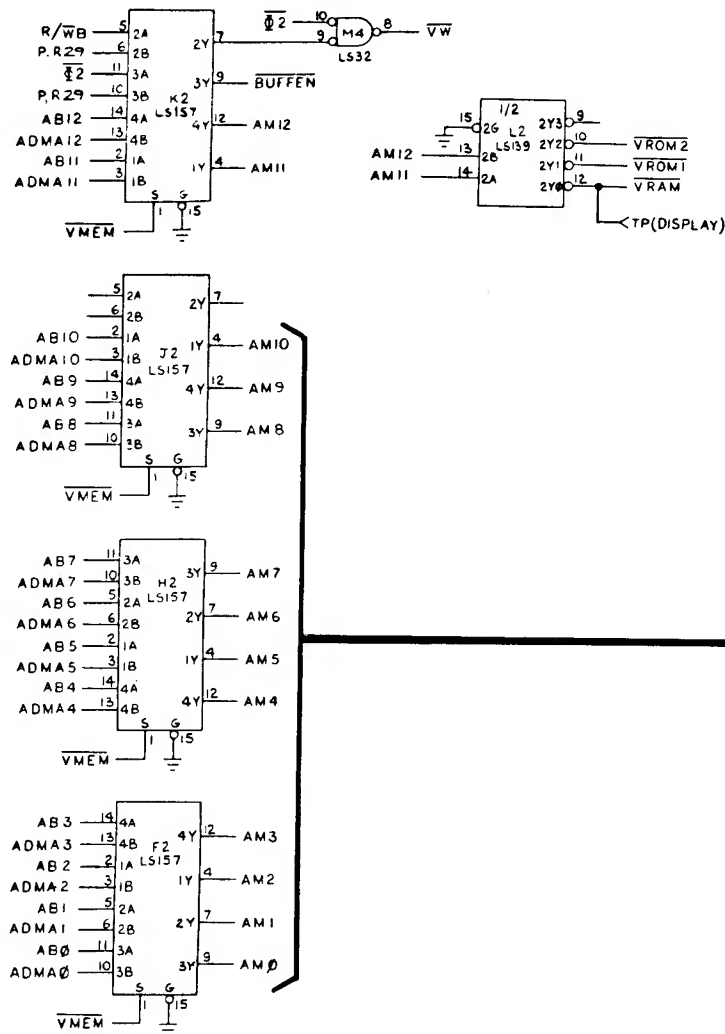
## STATE MACHINE



FROM  
MICROCOMPUTER  
SHEET 1, SIDE B

## VECTOR GENERATOR MEMORY ADDRESS SELECTOR

VECTOR

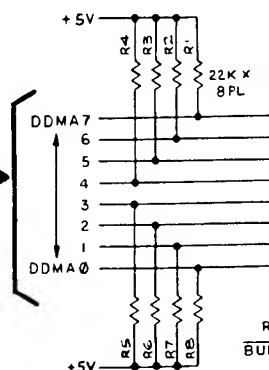


The address selector consists of multiplexers F2, H2, J2 and K2. When  $\overline{VMEM}$  is low, the MPU of the microcomputer gains access to the address inputs of the vector generator memory. In this state,  $\overline{BUFFEN}$  is from  $\overline{\Phi}2$  and  $\overline{VW}$  (vector generator write) is low when  $\overline{\Phi}2$  and  $\overline{R/WB}$  are both low. When  $\overline{VMEM}$  is high, the address input to the vector generator memory is from the vector generator program counter and state machine. In this state,  $\overline{BUFFEN}$  and  $\overline{VW}$  are both held high by the pullup resistors connected to the 2B and 3B inputs of multiplexer K2.

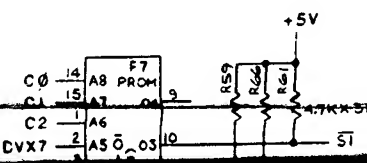
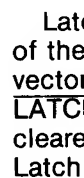
Address decoder L2 decodes address bits A11 and A12, and selects the RAM or one of three ROMs of the vector-generator memory.

This address-selecting arrangement allows the game MPU to access the vector-generator memory, i.e., write data into the vector-generator RAM to instruct the vector generator what it should do next. The address selector can then allow the vector-generator program counter and state machine to access this same area of RAM also, and read what instructions were sent to it by the game MPU.

## VECTOR GENERATOR DATA BUFFER



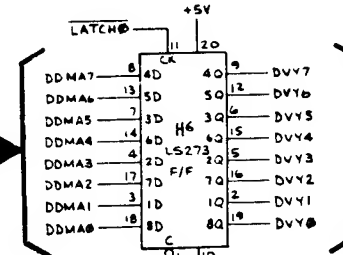
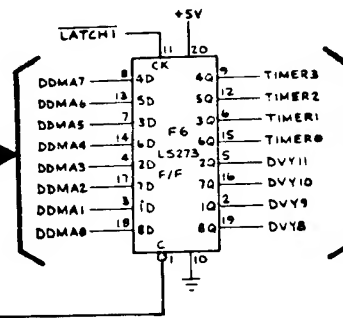
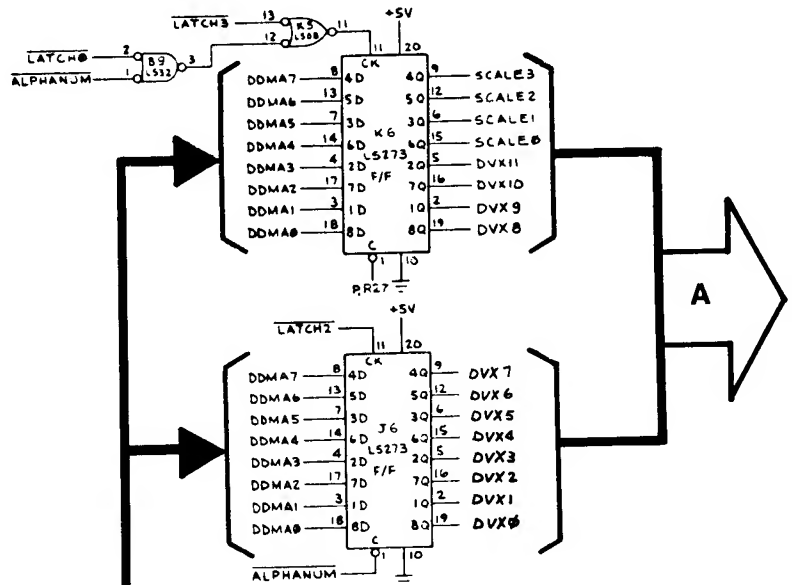
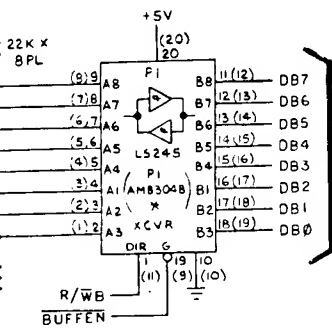
The latch 3 are the



OR

TO/FROM  
MPU DATA BUS  
SHEET 1, SIDE B

# VECTOR GENERATOR MEMORY DATA LATCHES



The data latches consist of latch 0 (H6), latch 1 (F6), latch 2 (J6), and latch 3 (K6). Inputs DDMA0 thru DDMA7 are the data outputs from the vector-generator memory.

Latches 0 thru 2 are directly clocked by the rising edge of the LATCH0, LATCH1, and LATCH2 outputs from the vector generator's state machine. Latch 3 is clocked by LATCH3 or by LATCH0, if ALPHANUM is low. Latch 0 is cleared when RESET, DMAGO, or ALPHANUM goes low. Latch 1 is cleared by ALPHANUM.

